CPS311 - COMPUTER ORGANIZATION

Professor:	Russell C. Bjork russell.bjork@gordon.edu	Fall Semester, 2015
Office:	KOSC 242 x4377	MWF 9:10-10:10 am KOSC 125
Hours:	MWF 2:10-3:10 pm; Tu 9-12 am and by appointment	Lab L1: R 9:45am-12:45pm Lab L2: R 1:15-4:15 pm Both in KOSC 241 and 244 (beginning 9/3)
Course Site:	Blackboard site and http://www.cs.gordon.edu/courses/cps311	

PREREQUISITE: Computer Science 122

CATALOG DESCRIPTION:

Introduces computers as physical devices composed of gates, binary representation of information, and the assembly-language level of computer description. Methods of improving performance including various forms of parallelism in hardware.

COURSE OBJECTIVES:

In general, this course is intended to familiarize you with the fundamental building blocks of modern computer systems, and with the way that computer systems are built up from the fundamental building blocks to form complete systems. The goal is not to have you learn how to design a computer system, but rather to help you become a more knowledgable user of computer hardware. In particular, upon completion of this course you should be able to

1. Explain the levels of computer structure.
2. Carry out the rudiments of digital logic design.
3. Convert between decimal, binary, and hexadecimal representations for numbers.
4. Discuss methods for representing other sorts of information (e.g. text, sounds, graphics, and more complex data structures) using binary numbers.
5. Describe the implementation of basic arithmetic operations by hardware.
6. Describe the architecture, organization and major components of a typical "Von Neumann architecture" computer.
7. Describe a typical RISC architecture (MIPS).
8. Write and run simple programs in MIPS assembly language.
9. Describe the implementation of basic instruction-set level functionality by means of register-transfer level operations.
10. Describe the organization of a RISC CPU
11. Describe the structure of the system bus and the memory and I/O subsystems.
12. Interface IO devices to a simple microprocessor bus system.
13. Describe various hardware mechanisms for supporting parallelism.
14. Describe how GPUs can be used for general-purpose computation
15. Discuss the measurement of computer system performance

TEXTS: Harris, David and Sarah. *Digital Design and Computer Architecture* 2nd ed. (Waltham, MA: Morgan Kauffman, 2013)

Custom book - order from http://academicpub.sharedbook.com/serve/ac/acapub/student_product_page.html?slug=1437408773_2_169

COURSE TECHNIQUES AND PROCEDURES

The primary goal of this course is for you to gain familiarity with the architecture and implementation of a modern computer, in order to be able to more intelligently purchase / use / develop software for such a machine. We will draw many of our examples from the MIPS architecture and implementation (a contemporary commercial architecture). However, our goal is not to become familiar with this particular architecture per se, but rather to become familiar with computer architecture at the instruction-set level, and how these capabilities are actually implemented in hardware.

As with other Computer Science courses, much of the learning will take place in the laboratory as you develop the various skills listed in the Course Objectives. Some of the laboratory sessions will focus on software - specifically machine and assembly language programming. Other laboratories will be hardware-oriented, both at the individual chip level early in the course, and through the use of a one-board computer.

In view of the complexity of some of the material, it is absolutely imperative that you keep up on your reading and your homework, and that you come to class prepared to ask questions about things you don't understand. Prior to each class period you should carefully read the assigned material in the textbook. Because the material is more technical than in some courses, you will probably find a greater than normal need to obtain personal help from the instructor. Please feel free to seek this.

COURSE REQUIREMENTS AND EVALUATION:

1. You will be expected to read material from the textbook, as assigned in the schedule below. Reading assignments should be completed **before** the class hour in which the topic is discussed. Lecture presentations will assume that you have read the text, and it is expected that your participation in the class will reflect that fact. However, our classroom discussion will not rigidly follow the order of material in the text, nor will it be confined to material covered there.

2. Eight problem sets will be posted on Blackboard during the semester, and will be due as shown in the course schedule. Note that these will be fairly substantial assignments; you would do well to work on the problems as the material is covered in class, rather than waiting until just before the set is due to tackle the whole assignment. Solutions to each problem set will be discussed in class and/or posted on Blackboard after the set is graded. Problem sets will be worth 30% of the final course grade. Credit for problem sets will be awarded on the basis of the completeness and correctness of your solutions, with significant credit given for a reasonably complete attempt at solving each problem, even if the final answer is not correct.

   The tentative emphases of the various problem sets are as follows *(subject to change.)*

Set	Emphases
1	Course Introduction; Combinatorial Logic
2	Sequential Circuits
3	Data Representations; Error Detecting and Correcting Codes
4	Machine and Assembly Language Programming
5	CPU Architectural Alternatives
6	CPU Internals; Control; Pipelining
7	The Memory System
8	The IO System; Parallel Hardware; Performance

Solutions to the odd numbered problems in the Harris text can be found online at http://booksite.elsevier.com/9780123944245/DDCAarm_solutions_odd.pdf. You may find a solution to an odd-numbered problem that is similar to one of the ones assigned helpful.

The following guidelines should be observed when doing these problem sets

- Homework sets will be due at the start of class on the date indicated. **Late homework will be accepted up until the time the graded homework is returned, for a 50% grade penalty, but NOT after that.**
- Homework sets must be done on one side only of 8-1/2 x 11 paper, and pages must be stapled in problem-number order. Problems must be numbered, and final answers (where appropriate) should be highlighted. (Homework sets not conforming to these standards will be returned ungraded.)
- You may work together with another student on homework, provided each of you works on each problem.
- Where an exercise calls for writing a program, it is sufficient to write it out by hand; you need not enter it into the computer.

3. Weekly laboratories will focus on gaining practical experience with the material covered in the book and/or in lecture. Lab assignments will be posted on Blackboard, and **must** be read over carefully **before** coming to lab.

   For each laboratory, there will be a writeup to turn in. One of the labs will run for two weeks, with everything due the second, but will be counted as two labs in grade computation. There may also be a quiz given at the start of the lab hour (based on your reading of the lab assignment) and/or a quiz based on the work done in lab given at the start of class on the due date. Each laboratory writeup and quiz(zes) will be worth 2% of the final course grade. (26% total for the 13 labs).

   The tentative emphases for the lab sessions is shown in the course schedule below *(subject to change)*.

4. A Computer-Aided Instruction program called BINARY will be made available for you to run. It is designed to give you thorough drilling in the use of binary, octal and hexadecimal representations of information. (Mastery of these representations is absolutely vital.) You may earn up to 100 points by completing the various drills quickly and accurately. You may repeat the drills as often as you like, and you will receive credit for the highest score attained on each of the topics prior to 4:00 pm on the due date. (You may continue working on the drill after then - but any additional points you earn will be for your own satisfaction only.) You may **NOT** use a calculator while doing these drills. This exercise will be worth 4% of the final course grade.

5. A mid-term examination (worth 20% of the final course grade) and a final examination (worth 20%) will be given as shown in the course schedule. Each exam will assume familiarity with material in the text, covered in lecture, and/or used in homework problems or the project. Exams will be open book (course text only), open notes.

6. Your final grade will be computed on the basis of a weighted sum of the items listed above.

Summary:	Problem Sets	30%
	Labs	26%
	Binary Drills	4%
	Exams	40%
		100%

The following are minimum guaranteed grades for the percentages indicated:

	93% - 100%: A	90% - 92.9%: A-
87% - 89.9%: B+	83% - 86.9%: B	80% - 82.9%: B-
77% - 79.9%: C+	73% - 76.9%: C	70% - 72.9%: C-
67% - 69.9%: D+	63% - 66.9%: D	60% - 62.9%: D-

POLICY STATEMENT ON EXTENSIONS AND INCOMPLETES:

1. Extensions of the due dates for homework or projects will be given in the event of extenuating circumstances (such as illness, personal emergency) IF you submit a brief written request to the professor as soon as possible after the circumstances arise. This request will be initialed (if approved) and will be returned to you. You must attach it to the piece of work for which the extension was granted.

2. A grade of Incomplete will be given without penalty IF you are unable to complete the course work by the last day of the term due to major illness or other similar emergency. Again, a written request should be submitted. Such a request will only be granted if you are substantially up-to-date with your course work and were making good progress in the course up to the time that the difficulty arose. Of course, you must complete all work for the course by the midpoint of the next semester in accordance with College policy.

3. A grade of Incomplete with a penalty of one letter grade to be applied in the final grade computation MAY be given if you are unable to complete all the course work for reasons other than those noted above. You must make a written request, and your progress in the course, class attendance etc. will be taken into consideration in determining whether to grant it. Again, you must complete all work for the course by the midpoint of the next semester.

ATTENDANCE POLICY:

Regular class attendance is expected of all students, and class attendance will be recorded. Absences from class will be classified as "documented" or "undocumented". A documented absence is one where written documentation is submitted supporting an absence from class due to circumstances beyond the student's control. An undocumented absence is any other absence, including one which could qualify as documented if proper documentation were submitted.

Students who have more than three undocumented absences during the semester should expect to see their final grade reduced by 1% for each undocumented absence over 3, and students who have more than 12 undocumented absences will fail the course automatically. The allowance of 3 undocumented absences may be reduced by one for each documented absence over 3 - e.g. a student who has 2 documented absences may be allowed only 1 undocumented absence without

grade penalty. (This will not be applied retroactively, though) Note that it is not necessary to document absences unless there are more than three total absences; for most students, this will avoid the need to submit documentation. A student who anticipates the need to miss more than three classes due to athletic competitions or other student activities should review the college's attendance policy in the catalog, and should then discuss alternatives to class attendance with the professor at the start of the semester.

A student who is habitually late will have late arrival for class counted as a half absence for that class, and a student who sleeps through most or all of a given class session will be counted as absent for that class.

You may ask the professor to waive this policy for you if you earned an A in the prerequisite course, or if you have an A average in this course as of the mid-term exam. If you wish to take advantage of this exemption, you must so inform the professor. However, the attendance policy will be reimposed if your subsequent work deteriorates.

ACCOMMODATION FOR STUDENTS WITH DISABILITIES:

Gordon College is committed to assisting students with documented disabilities (see Academic Catalog Appendix C, for documentation guidelines). A student with a disability who may need academic accommodations should follow this procedure:

1. Meet with a staff person from the Academic Support Center (Jenks 412 X4746) to:
   a. make sure documentation of your disability is on file in the ASC,
   b. discuss the accommodations for which you are eligible,
   c. discuss the procedures for obtaining the accommodations, and
   d. obtain a **Faculty Notification Form**.

2. Deliver a Faculty Notification Form to each course professor *within the first full week of the semester;* at that time make an appointment to discuss your needs with each professor.

Failure to register in time with your professor and the ASC may compromise our ability to provide the accommodations. Questions or disputes about accommodations should be immediately referred to the Academic Support Center. See Grievance Procedures available from the ASC.

TENTATIVE COURSE SCHEDULE

Date	**Topic(s)**	**Reading**	**Written Work Due**
		(All in main text by Harris unless otherwise stated)	
W 8/26	Course Introduction; The Levels of Computer Structure; Architecture and Organization		
R 8/27	*(Lab doesn't start until 9/3)*		
F 8/28	Levels, etc. (continued)	§1.1-1.3	
M 8/31	Introduction to Digital Logic: Combinatorial Logic	§1.5, 2.1	**START PROBLEM SET 1**
W 9/2	(continued)	§2.2-2.7	
R 9/3	Lab: Levels of Computer Structure (1) KOSC 241		
F 9/4	Combinatorial Logic (continued)	§2.8; §1.6, 1.8; §2.9-2.10; §5.1-5.2 through top of p. 241	**LAB 1 DUE**
M 9/7	*Labor Day - no class*		
W 9/9	Sequential Logic	§3.1-3.2	
R 9/10	Lab: Realizing Boolean expressions with TTL SSI gates (2) KOSC 241		
F 9/11	Sequential Logic (continued)	§3.4	**LAB 2 DUE**
M 9/14	(continued)	§3.6-3.7	**PROBLEM SET 1 DUE**
W 9/16	Representing Information in Binary	§1.4	
R 9/17	Lab: Sequential Circuits (3) KOSC 244		
F 9/18	Binary Representation (continued)	§5.3	**(One writeup due next week for Labs 3 and 4)**
M 9/21	Error Detecting and Correcting Codes		**PROBLEM SET 2 DUE**
W 9/23	Introduction to the MIPS Architecture and Assembly Language	§6.1-6.3; §6.7.3; MIPS ISA Handout	
R 9/24	Lab: Sequential Circuits ctd (4) KOSC 241		
F 9/25	MIPS Architecture (continued)		**LABS 3-4 DUE**
M 9/28	Control Structures; MIPS Branch and Jump Instructions	§6.4.1-6.4.5; Control Structures Handout	**PROBLEM SET 3 DUE; START BINARY DRILLS**
W 9/30	(continued)		

R 10/1	Lab: MIPS Machine and Assembly Language (5) KOSC 244		
F 10/2	Procedures and Parameter Passing	§6.4.6; MIPS Procedures Handout	**LAB 5 DUE**
M 10/5	(continued)		
W 10/7	Exceptions and Interrupts	§6.7.2; Exception-Handling Handout	
R 10/8	Lab: Using the MIPS Assembler and Debugger (6) KOSC 244		
F 10/9	Other CPU Architectures: 0, 1, 2 and 3 address machines; addressing modes; CISC's vs RISC's	§6.5, 6.8	**LAB 6 DUE**
M 10/12	(continued)		**PROBLEM SET 4 DUE**
W 10/14	Review and Catch Up		
R 10/15	*No lab - quad break*		
F 10/16	*No class - quad break*. Binary Drills due by 4 PM		**BINARY DRILLS DUE**
M 10/19	**MIDTERM EXAM (THROUGH EXCEPTIONS AND INTERRUPTS)**		
W 10/21	CPU Implementation; The Register Transfer Level; Internal Busses and the ALU	§5.2.2-5.2.5; §7.1	
R 10/22	Lab: Data Structures and Addressing Memory (7) KOSC 244		
F 10/23	CPU Implementation (continued)		**LAB 7 DUE**
M 10/26	Control Unit Implementation: Hardwired and Microprogrammed Control	§7.3-7.4	
W 10/28	Pipelining; Superscalar Computers; Instruction-Level Parallelism	§7.5	**PROBLEM SET 5 DUE**
R 10/29	Lab: Procedures; Recursion (8) KOSC 244		
F 10/30	Pipelining (continued)	§7.8	**LAB 8 DUE**
M 11/2	Memory Devices	§5.5-5.5.6	
W 11/4	(continued)		
R 11/5	Lab: Data Paths and MUXes (9) KOSC 244		
F 11/6	Memory Devices (continued)		**LAB 9 DUE**
M 11/9	Memory Hierarchies	§8.1-8.3	**PROBLEM SET 6 DUE**
W 11/11	(continued)	§8.4	

R 11/12	Lab: Control Units (10) KOSC 244		
F 11/13	Memory Hierarchies (continued)	§8.8-8.9	**LAB 10 DUE**
M 11/16	(continued)		
W 11/18	the Input-Output Subsystem; Bus Structures; Interrupts and DMA	§8.5, quickly skim §8.6-§8.7	
R 11/19	Lab: Memory Devices (11) KOSC 241		
F 11/20	(continued)		**LAB 11 DUE**
M 11/23	(continued)		**PROBLEM SET 7 DUE**
W 11/25	*Thanksgiving Break - no class*		
R 11/26	*Thanksgiving Break - no lab*		
F 11/27	*Thanksgiving Break - no class*		
M 11/30	IO (continued)		
W 12/2	Hardware Support for Parallelism	Custom Book §6.1-6.8	
R 12/3	Lab: IO Interfacing (12) KOSC 241		
F 12/4	Hardware Support for Parallelism (continued)		**LAB 12 DUE**
M 12/7	Performance Measurement and Analysis	§7.2; Wikipedia article: http://en.wikipedia.org/wiki/Benchmark_(computing)	
W 12/9	Review and Catch Up		
R 12/10	Lab: Parallel Computing (13) KOSC 244		
F 12/11	*No class - Reading Day*. Lab and Homework due by 4 PM		**LAB 13 DUE; PROBLEM SET 8 DUE**

WEDNESDAY, DECEMBER 16 - 9:00-11:00 AM - FINAL EXAM